Customer No. 22,852
Attorney Docket No. 04329.3151

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Katsuhiko HIEDA et al.	Group Art Unit: Not Yet Assigned
Serial No.: Not Yet Assigned	Examiner: Not Yet Assigned
Filed: October 1, 2003	
For: METHOD FOR MANUFACTURING A SEMICONDUCTORDEVICE	

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants

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reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: October 1, 2003

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OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3151	Serial No.	Not Yet Assigned
Applicants	Katsuhiko HIEDA et al.		
Filing Date	October 1, 2002	Group:	Not Yet Assigned

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,191,002	02/20/01	Koyanagi			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Heo et al., "Void Free and Low Stress Shallow Trench Isolation Technology Using P-SOG For Sub 0.1 *μm* Device", 2002 Symposium On VLSI Technology Digest of Technical Papers, pp. 132-133, 2002.

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce